Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	SOI and (insulator or insulating or insulative or dielectric) and etching and rinsing and (solution same spheres)	US-PGPUB; USPAT	OR	ON	2005/11/21 15:02
L2	1	SOI and (insulator or insulating or insulative or dielectric) and etching and rinsing and (solution same spheres)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:04
L3	1	(igor adj gory) or (bruce adj gnade) or (fadizso adj mantiziba)	US-PGPUB; USPAT	OR	ON	2005/11/21 14:06
L4	0	(igor adj gory) or (bruce adj gnade) or (fadizso adj mantiziba)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:06
L5	127	zyvex	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:07
L6	39	5 and solution	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:09
L7	3	6 and (SOI or (insulator adj on adj substrate))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:08
L8	36	6 not 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:09
L9	214	SOI and (insulator or insulating or insulative or dielectric) and etching and rinsing and (solution)	US-PGPUB; USPAT	OR	ON	2005/11/21 14:28
L10	171	9 and @ad<"20031007"	US-PGPUB; USPAT	OR	ON	2005/11/21 14:37
L11	5377	SOI and (insulator or insulating or insulative or dielectric) and etching and (solution)	US-PGPUB; USPAT	OR	ON	2005/11/21 14:29
L12	148	11 and (micro with electronic)	US-PGPUB; USPAT	OR	ON	2005/11/21 14:29

L13	100	12 and @ad<"20031007"	US-PGPUB; USPAT	OR	ON	2005/11/21 14:37
L14	96	13 not 10	US-PGPUB; USPAT	OR	ON	2005/11/21 14:29
L15	237	438/22,24,48,106,110,115.ccls. and SOI and (insulator or insulating or insulative or dielectric)	US-PGPUB; USPAT	OR	ON	2005/11/21 14:36
L16	184	15 and @ad<"20031007"	US-PGPUB; USPAT	OR	ON	2005/11/21 14:36
L17	181	16 not 10	US-PGPUB; USPAT	OR	ON	2005/11/21 14:37
L18	179	17 not 13	US-PGPUB; USPAT	OR	ON	2005/11/21 14:37
L19	1	((SOI or (insulator adj on adj substrate)) and (insulator or insulating or insulative or dielectric) and (etch or etching) and (micro adj electronic) and (solution or slurry)).clm.	US-PGPUB; USPAT	OR	ON	2005/11/21 14:39
L20	1	SOI and (insulator or insulating or insulative or dielectric) and etching and rinsing and (slurry same spheres)	US-PGPUB; USPAT	OR	ON	2005/11/21 15:03
L21	1	SOI and (insulator or insulating or insulative or dielectric) and etching and (slurry same spheres)	US-PGPUB; USPAT	OR	ON	2005/11/21 15:03
L22	2	SOI and (insulator or insulating or insulative or dielectric) and etching and (slurry same spherical)	US-PGPUB; USPAT	OR	ON	2005/11/21 15:04
L23	7	SOI and (insulator or insulating or insulative or dielectric) and etching and (solution same spherical)	US-PGPUB; USPAT	OR	ON	2005/11/21 15:05
L24	1	SOI and (insulator or insulating or insulative or dielectric) and etching and (solution same spherical)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:05
L25	1	SOI and (insulator or insulating or insulative or dielectric) and etching and (slurry same spherical)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:14
L26	0	SOI and (insulator or insulating or insulative or dielectric) and etching and (slurry same spherically)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:14

L27	297	SOI and (insulator or insulating or insulative or dielectric) and etching and ((colloid or slurry or suspension or suspended) same particles)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:16
L28	56	27 and (mems or (micro with device))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:16

DOCUMENT-IDENTIFIER: US 20030159644 A1

TITLE: METHOD OF MANUFACTURING SEMICONDUCTOR WAFER METHOD OF
USING AND UTILIZING THE SAME

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Summary of Invention Paragraph - BSTX (14):
[0013] Then, the porous layer 4B remaining on the surface of the epitaxial layer 5 that has been transferred to the second semiconductor wafer 2 (also referred to as handle wafer or base wafer) is removed by wet etching, using a mixture **solution** of hydrofluoric acid and hydrogen peroxide. Then, as shown in FIG. 17E, the exposed epitaxial layer is smoothed typically by hydrogen annealing to produce a finished SOI that has remarkable characteristics.

Summary of Invention Paragraph - BSTX (15):
[0014] On the other hand, the separated Si wafer still maintains the profile of a thin disk. Therefore, it can be used as Si wafer 1 for preparing another SOI wafer as shown in FIG. 17A for another time after removing the porous layer remaining on the cleaved side thereof also by wet etching, using the same **solution**. Alternatively, it may be used as semiconductor wafer 2 for preparing another SOI wafer as shown in FIG. 17B.

Detail Description Paragraph - DETX (22):
[0094] As a polishing method, chemical and mechanical polishing (CMP) is preferred. As a polishing agent for performing CMP, there can be employed silica glass (borosilicate glass), titanium dioxide, titanium nitride, aluminum oxide, iron nitrate, cerium oxide, colloidal silica, silicon nitride, silicon carbide, graphite, polishing granule such as diamond, or a granule liquid having these granules and oxidizing agent such as H.sub.2O.sub.2 or KIO.sub.3 or alkali **solution** such as NaOH, KOH or the like mixed therewith.

Detail Description Paragraph - DETX (26):
[0098] Making it porous for forming a separation layer is conditionally possible on a N-type semiconductor, and however, it is desirable to employ a P-type semiconductor. Unagami et al. studied Si **solution** reaction in anodization, and concluded that positive pores were required in anodization in HF **solution** (T Unagami, J. Electrochem. Soc., vol. 127,476 (1980)). To make it porous, a high concentration P-type semiconductor wafer is preferably

employed, and its impurities concentration range is generally from 5.0.times.10.sup.16/cm.sup.3 to 5.0.times.10.sup.20/cm.sup.3, preferably 1.0.times.10.sup.17/cm.sup.3 to 2.0.times.10.sup.20/cm.sup.3, and more preferably, 5.0.times.10.sup.17/cm.sup.3 to 1.0.times.10.sup.20/cm.sup.3. When a separation layer is formed by ion plantation, hydrogen, nitrogen, rare gas or the like (He, Ne, Ar or the like) is employed as an ion implantation species. At least one or more of them may be implanted.

Detail Description Paragraph - DETX (132):
[0204] When a plurality of first substrates are disposed in an anodization **solution** to form a porous layer, a silicon wafer has been disposed on the anode side as a shield wafer in order to prevent the deposition of a metal ion eluted from the anode to the back side of the first substrate. When two or more porous layers are formed by changing a current density, a similar structure may be formed on the surface of a shield wafer. If such shield wafer is used n-times, a 2 n-layered porous layer is formed in the shield wafer. The porous layer becomes extremely unstable. For example, a porous portion formed at the shield wafer has been peeled off at n+1 times, and sometimes has diffused in a container. In particular, when the lowly and highly porous layers are formed alternately, the mechanical strength is lowered more significantly than a case in which a porous layer having the same thickness is formed under constant forming conditions. That is, use of the shield wafer has been limited. However, according to the present invention, a two or more layered structure of the porous layer of the first substrate is determined depending on a structure of the epitaxially grown layer formed in advance on the surface of the first substrate. Thus, the density of current to be applied to the shield wafer can be made constant, and the service life of the shield wafer can be extended.

Detail Description Paragraph - DETX (183):
[0254] A first p-type monocrystalline Si substrate showing a specific resistance between 0.01 and 0.02 .OMEGA..multidot.cm was anodized in an HF **solution**.

Detail Description Paragraph - DETX (204):
[0274] A first p-type monocrystalline Si substrate showing a specific resistance between 0.01 and 0.02 .OMEGA..multidot.cm was anodized in an HF **solution**.

Detail Description Paragraph - DETX (220):
[0289] P-type monocrystalline Si showing a specific resistance of 0.015 .OMEGA..multidot.cm was formed on a first monocrystalline Si substrate to a thickness of 15 .mu.m by epitaxial growth, using a CVD technique and then

anodized from the surface of the substrate in an HF **solution**.

Detail Description Paragraph - DETX (231):
[0299] P-type monocrystalline Si showing a specific resistance of 0.015 .OMEGA..multidot.cm was formed on a first monocrystalline Si substrate to a thickness of 16 .mu.m by epitaxial growth, using a CVD technique and then anodized from the surface of the substrate in an HF **solution**.

Detail Description Paragraph - DETX (267):
[0331] A first p-type monocrystalline Si substrate showing a specific resistance between 0.01 and 0.02 .OMEGA..multidot.cm was anodized in an HF **solution**.

Detail Description Paragraph - DETX (279):
[0342] A first p-type monocrystalline Si substrate showing a specific resistance of 0.01 .OMEGA..multidot.cm was anodized in an HF **solution**.

Detail Description Paragraph - DETX (291):
[0353] Then, the epitaxial layer was anodized in a mixture **solution** of HF and ethanol.

Detail Description Paragraph - DETX (294):
[0356] The wafer was then treated at 400.degree. C. for an hour in an oxygen atmosphere and immersed into a 1.25% aqueous **solution** of HF for 30 seconds to remove the very thin silicon oxide film on the surface. Then, the wafer was put into an epitaxial growth apparatus to produce a 0.3 .mu.m thick monocrystalline Si layer by epitaxial growth, using a CVD (chemical vapor deposition) technique. The conditions of the epitaxial growth are listed below. Note that the above described hydrogen baking process, the process of supplying a small amount of raw material and the high temperature baking process may be conducted prior to the process of growing monocrystalline Si.

Detail Description Paragraph - DETX (297):
[0359] The bonded wafers were forcibly separated along the highly porous layer. Various techniques may be used to separate them apart including application of pressure, application of tensile or shearing force, application of external pressure by means of a wedge, application of ultrasonic waves, application of heat, generating internal pressure within the porous Si layer by causing it to expand through oxidation, application of a pulse of heat to generate thermal stress in the inside and softening. As a matter of fact it was possible to separate them by any of the above listed techniques. Subsequently, the support substrate was immersed into an aqueous **solution** of a

mixture of HF and hydrogen peroxide to find that the residual porous silicon layer was removed from the surface in about 60 minutes to produce an SOI wafer.

Detail Description Paragraph - DETX (301):
[0363] The residual porous layer on the first substrate was immersed into an aqueous **solution** of a mixture of HF and hydrogen peroxide to find that it was removed in about 30 minutes. The 1 .mu.m thick epitaxial layer on the first p-type monocrystalline Si substrate was then subjected to hydrogen annealing to reduce the impurity concentration. Then, the substrate was used to prepare a CMOS logic circuit.

Detail Description Paragraph - DETX (306):
[0367] Then, the epitaxial layer was anodized in a mixture **solution** of HF and ethanol.

Detail Description Paragraph - DETX (309):
[0370] The wafer was then treated at 400.degree. C. for an hour in an oxygen atmosphere and immersed into a 1.25% aqueous **solution** of HF for 30 seconds to remove the very thin silicon oxide film on the surface. Then, the wafer was put into an epitaxial growth apparatus to produce a 0.3 .mu.m thick monocrystalline Si layer by epitaxial growth, using a CVD (chemical vapor deposition) technique. The conditions of the epitaxial growth are listed below. Note that the above described hydrogen baking process, the process of supplying a small amount of raw material and the high temperature baking process may be conducted prior to the process of growing monocrystalline Si.

Detail Description Paragraph - DETX (313):
[0374] Subsequently, the support substrate was immersed into an aqueous **solution** of a mixture of HF and hydrogen peroxide to find that the residual porous silicon layer was removed from the surface in about 60 minutes to produce an SOI wafer.

Detail Description Paragraph - DETX (317):
[0378] The residual porous layer on the first substrate was immersed into an aqueous **solution** of a mixture of HF and hydrogen peroxide to find that it was removed in about 30 minutes. Then, an epitaxial layer was made to grow with a boron concentration lower than that of the first p-type monocrystalline Si substrate in order to produce an epi-wafer. The epi-wafer was used to prepare a CMOS logic circuit.

Detail Description Paragraph - DETX (342):
[0400] The surface of a first monocrystalline Si substrate was subjected to

an anodization process in an HF **solution**.

Detail Description Paragraph - DETX (355):
[0413] The porous Si remaining on the first substrate was selectively etched out by immersing it into an aqueous **solution** of a mixture of 49% hydrofluoric acid and 30% hydrogen peroxide to produce a bulk wafer having a smooth surface. It was used as a device forming wafer or a monitor wafer without being used as first or second substrate as described above.

Detail Description Table CWU - DETL (1):
1 current density: 7 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 11 (minutes) thickness of porous Si: 12 (.mu.m)

Detail Description Table CWU - DETL (3):
3 current density: 7 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 5 (minutes) thickness of porous Si: 5.5 (.mu.m)

Detail Description Table CWU - DETL (5):
5 current density: 7 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 11 (minutes) thickness of porous Si: 12 (.mu.m) current density: 22 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 2 (minutes) thickness of porous Si: 3 (.mu.m)

Detail Description Table CWU - DETL (7):
7 current density: 7 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 11 (minutes) thickness of porous Si: 12 (.mu.m) current density: 22 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 2 (minutes) thickness of porous Si: 3 (.mu.m)

Detail Description Table CWU - DETL (11):
11 current density: 7 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 11 (minutes) thickness of porous Si: 12 (.mu.m)

Detail Description Table CWU - DETL (13):
13 current density: 7 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 12 (minutes) thickness of porous Si: 11 (.mu.m)

Detail Description Table CWU - DETL (15):
15 current density: 7 (mA .multidot. cm.sup.2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 12 (minutes)

Detail Description Table CWU - DETL (17):
17 current density: 7 (mA .multidot. cm.sup.2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 4 (minutes)

Detail Description Table CWU - DETL (21):
21 current density: 1 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 0.1 (minutes) thickness of porous Si: 0.02 (.mu.m)

Detail Description Table CWU - DETL (22):
22 current density: 50 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 5 (seconds) thickness of porous Si: 0.1 (.mu.m)

Detail Description Table CWU - DETL (23):
23 current density: 7 (mA .multidot. cm.sup.-2) anodizing **solution**: HF:H.sub.2O:C.sub.2H.sub.5OH = 1:1:1 time: 1 (minutes) thickness of porous Si: 1 (.mu.m)

DOCUMENT-IDENTIFIER: US 20010031514 A1

TITLE: Method and apparatus for fabricating self-assembling microstructures

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Summary of Invention Paragraph - BSTX (17):
[0017] In an alternative embodiment, the method provides, for example, shaped blocks having a trapezoidal profile from an improved fabrication process. Fabrication includes providing a second substrate having a top surface, and growing a sacrificial layer overlying the top surface. A step of forming a block layer overlying the top surface is then performed. Masking and etching the block layer up to the sacrificial layer creates trapezoidal shaped blocks thereon. A step of preferential etching the sacrificial layer lifts off each trapezoidal shaped block. Such blocks are then rinsed and transferred into a **solution** forming the slurry. In this embodiment, the method provides alternate fabrications of the shaped blocks. One such alternate fabrication of the shaped blocks includes providing a second substrate as a block layer having an upper surface and a bottom surface, and growing a sacrificial layer overlying the upper surface. Another alternative fabrication of the shaped blocks includes providing a second substrate having an upper surface, a sacrificial layer overlying the upper surface, and a block layer overlying the sacrificial layer. After providing the second substrate, a step of forming trapezoidal shaped blocks on and in contact with the sacrificial layer is then performed. The trapezoidal shaped blocks are then removed from contact with the sacrificial layer, and transferred into a fluid to form a slurry.

Detail Description Paragraph - DETX (3):
[0045] In the assembly of a gallium arsenide block onto a silicon wafer, trapezoidal shaped blocks self-align into inverted trapezoidal shaped recessed regions located on the top surface of the silicon wafer. Steps for such method include forming the gallium arsenide blocks, transferring the blocks into a **solution** forming a slurry, and spreading the slurry evenly over the top surface of a silicon substrate having recessed regions. During the spreading steps, the blocks self-align and settle into the recessed regions while being transported with the fluid across the top surface. Optionally, the slurry is spread evenly over the top surface of a silicon substrate by way of mechanical means such as a brush, a scraper, tweezers, a pick, a doctor blade, and others. The mechanical means may be used to move or distribute the slurry and also to

remove excess slurry. As an alternative to spreading the slurry, the method includes circulating the slurry over the top surface of the substrate having recessed regions. During the circulating step, the blocks self-align and settle into the recessed regions while being transported with the fluid across the top surface. The blocks which do not settle into recessed regions are then recirculated until a certain fill-factor is achieved. Of course, the mechanical means may also be used in conjunction with the circulating step. The details of fabricating the silicon substrate having recessed regions will be discussed in detail below after a brief discussion of forming the gallium arsenide blocks. Details of the method using the circulating step and related apparatus will be discussed in detail below after a discussion of fabricating the silicon substrate having recessed regions.

Detail Description Paragraph - DETX (10):
[0052] In a specific embodiment, after etching the MBE grown layer, trapezoidal shaped blocks are removed through a lift-off technique from gallium arsenide substrate 10 by preferential etching sacrificial layer 13 as illustrated in FIG. 3. Such lift-off technique occurs by, for example, a preferential wet etch of the aluminum arsenide sacrificial layer. In the gallium arsenide example, such wet etching step is typically performed by a chemical such as a hydrofluoric acid **solution** or the like. The etchant used substantially etches the sacrificial layer but does not aggressively attack gallium arsenide blocks and/or substrates.

Detail Description Paragraph - DETX (11):
[0053] After separating the gallium arsenide blocks from substrate 10, methods of diluting and decanting the wet etchant **solution** remove the blocks from the **solution**. In the gallium arsenide example, the wet etchant is diluted and decanted using purified water, methanol, ethanol, or the like. Optionally, a rinsing step occurs after the diluting and decanting step. The rinsing step relies on solutions such as acetone, methanol, ethanol, or any other inert **solution** having low corrosive properties. Such **solution** also provides a medium (or fluid) for creating a mixture having blocks suspended therein or generally a slurry.

Detail Description Paragraph - DETX (12):
[0054] Instead of the lift-off technique illustrated in FIG. 3, an alternative lift-off method creates intermediate structure 250 of FIG. 4 from the gallium arsenide structure of FIG. 2a. Such alternative lift-off method also promotes lift-off of the shaped blocks in applications where the devices are formed onto the backside of the blocks. As shown, the method includes spreading a filler or wax layer 253 preferably high temperature wax overlying

the top surface of exposed portions of sacrificial layer 13 and gaps 255 between each block 19. One such wax includes a product by the name of TECH WAX made by TRANSENE Co., Inc. The method then includes inverting the gallium arsenide structure of FIG. 2a and attaching top surface 21 onto intermediate substrate 257. Such intermediate substrate is, for example, a silicon wafer or the like. However, prior to the attaching step, intermediate substrate surface 261 undergoes steps of etching off any native oxide preferably with a wet etchant such as hydrofluoric acid, and treating the cleaned surface with an adhesion promoter such as hexamethyldisilazane also called HMDS. In removing gallium arsenide substrate 10, backside 263 is lapped until about 50 .mu.m remains on substrate 10. The remaining thickness of substrate 10 is then etched up to aluminum arsenide layer 13. An etchant such as ammonium hydroxide and hydrogen peroxide (6:200 NH.sub.3OH:H.sub.2O.sub.2) preferentially etches the gallium arsenide substrate up to aluminum arsenide layer 13. Accordingly, the aluminum arsenide layer acts as an etch stop protecting gallium arsenide blocks 19. Removing aluminum arsenide layer 13 requires a step of wet etching using an etchant such as hydrofluoric acid. Such etchant typically removes aluminum arsenide layer 13 after a short dip in such **solution**. After the aluminum arsenide layer is completely removed, steps including masking, sputtering, and etching form metallized ring contacts 265 as illustrated in FIG. 5. Such metallized ring contacts were made by patterns formed from photoresist layer 267. The metallization for such contacts include materials such as gold, aluminum, among others. Alternatively, other processing steps such as etching, masking, implantation, diffusion, and the like may be performed on the blocks to create other profiles as well as active devices thereon. A **solution** such as trichloroethane (TCA) dissolves the filler or wax disposed between each block 19 and photoresist layer 21, and lifts off the gallium arsenide blocks 19 from intermediate substrate 257. To decrease corrosion, the gallium arsenide blocks are transferred to an inert **solution** such as acetone, methanol, ethanol, or any other **solution** having low corrosive characteristics. Such inert **solution** and blocks are often called a mixture or generally a slurry.

Detail Description Paragraph - DETX (16):

[0058] In the two preceding examples of forming trapezoidal shaped blocks from silicon, the slowest etching planes for silicon in the KOH:H.sub.2O **etching solution** used are the [111] planes, which can be considered etch stops forming the sloping sides of the shaped blocks. In each silicon example, the respective mask used to define the blocks must be aligned to the appropriate crystal axis. As shown in FIG. 20, a mask 850 was used to form the silicon trapezoidal blocks 855. Silicon trapezoidal shaped block 855 is formed at the intersection of the diagonal lines on mask 850, and the larger face 860 of silicon trapezoidal shaped block 855 is in contact with sacrificial layer (respectively 709 and 807, for the first and second preceding silicon examples). The width of the diagonal mask lines in FIG. 20 must be twice the thickness (t) of silicon block layer. For the larger silicon trapezoidal blocks, a=0.2 mm and silicon block layer 703 has t=235 .mu.m; whereas, for the smaller silicon trapezoidal blocks, a=0 and silicon block layer 809 has t=35 .mu.m.

Detail Description Paragraph - DETX (18):
[0060] In the first silicon example with the larger shaped blocks, the etched silicon wafer is placed in concentrated HF etch **solution** to remove the shaped blocks from contact with the SiN.sub.x sacrificial layer and any remaining SiN.sub.x from the mask layer. In the second silicon example with the smaller shaped blocks, the etched SOI wafer similarly is placed in concentrated HF etch **solution** to remove the shaped blocks from contact with the SiO.sub.2 sacrificial layer and any remaining SiN.sub.x from the mask layer. This HF etch **solution** preferentially etches the SiO.sub.2 and the SiNx to free the shaped blocks without etching the silicon shaped blocks. In particular, a HF **solution** having a concentration of about 1:1 HF:H.sub.2O was used to etch the sacrificial layer and residual SiNx to free the shaped blocks.

Detail Description Paragraph - DETX (19):
[0061] The slurry comprises an inert **solution** (of fluid) and shaped blocks. Enough **solution** exists in the slurry to allow the blocks to slide across the top surface of the substrate. Preferably, the amount of **solution** in the mixture is at least the same order as the amount of blocks. Of course, the amount of **solution** necessary depends upon characteristics such as block size, block material, substrate size, substrate material, and **solution**. After preparation, the slurry is transferred or spread over top surface 53 of silicon substrate 50 as illustrated in FIG. 6. The details of the transferring technique are discussed below after a brief discussion in fabricating silicon substrate 50.

Detail Description Paragraph - DETX (21):
[0063] The transferring technique includes a step of evenly spreading or pouring the slurry over top surface 53. The transferring technique may be accomplished by pouring a vessel of slurry evenly over top surface 53. Alternatively, the slurry may also be transferred from a pipet, flask, beaker, or any other type of vessel and/or apparatus capable of evenly transferring the slurry over top surface 53. Generally, the slurry is poured over top surface 50 at a rate which allows substantial coverage of the top surface, but prevents blocks already disposed into the recessed regions from floating or popping out.

Slurry flow is typically laminar but can be non-laminar, depending upon the particular application. In the gallium arsenide block example, the fluid flux over top surface 53 occurs at a velocity between about 0.01 mm/sec. and about 100 mm/sec. Preferably, fluid flux occurs at about 1 mm/sec. At such flux rates, the blocks flow evenly with the fluid, tumble onto top surface 53, self-align, and settle into recessed regions 55. Optionally, to prevent the blocks already disposed in the recessed regions from floating out, the transferring step may take place in a centrifuge or the like. A centrifuge, for example, places a force on the blocks already disposed in the recessed regions and thereby prevents such blocks from floating out with **solution**.

Detail Description Paragraph - DETX (38):

[0079] In a gallium arsenide example, a slurry including gallium arsenide blocks were transferred such that the blocks self-aligned into recessed regions located on a top surface of a silicon substrate. The steps for such method included forming the gallium arsenide blocks, transferring the blocks into a **solution** forming a slurry, and transporting the slurry evenly over a top surface of a silicon substrate having recessed regions. The shaped blocks generally tumble onto the top surface of the substrate, self-align and engage with a recessed region having a complementary shape.

Detail Description Paragraph - DETX (39):

[0080] In creating the silicon substrate, a **solution** of ethylenediamine pyrocatechol pyrazine (EDP) or potassium hydroxide (KOH) produced recessed regions having a trapezoidal profile or inverted truncated pyramid shape. Each **solution** created trapezoidal shaped profiles having an outward slope of about 55.degree. from an angle normal to the top surface of the substrate. Trapezoidal profiles occurred due to the selectivity (1:100) between the [111] plane and the [100] or [110] plane. Specifically, the [111] plane etched slower than the [100] or [110] plane by a ratio of 1:100.

Detail Description Paragraph - DETX (40):

[0081] In the present example, an EDP **solution** etched recessed regions into a silicon substrate. EDP includes ethylenediamine (about 500 ml.), pyrocatechol (about 160 gms.), water (about 160 gms.), pyrazine (about 1 gm.). The EDP bath was also at a temperature of about 115.degree. C. Prior to the etching step, a thermal oxide (SiO.sub.2) layer having a thickness of about 200 nm was first formed on a top surface of such substrate. Masking and etching such oxide layer formed rectangular shaped regions. Such regions were then etched vertically about 10 .mu.m forming square openings on the top surface about 23 .mu.m in length. Sides protrude down symmetrically from each opening to a square base having a length of about 9 .mu.m.

Detail Description Paragraph - DETX (47):

[0088] In addition to mask alignment, etchant concentration also affected the shape of each gallium arsenide block. A **solution** of phosphoric acid, hydrogen peroxide, and water (H.sub.2PO.sub.3:H.sub.2O.sub.2:H.sub.2O) provided a promising etchant for the MBE grown gallium arsenide layer in the present example. Such etchant created three distinct profiles, depending upon the amount of hydrogen peroxide and water added to phosphoric acid. Dilute concentrations of phosphoric acid (1:1:40 H.sub.2PO.sub.3:H.sub.2O.sub.2:H.sub.2O) created a trapezoidal or mesa shaped profile having a 30.degree. angle between the top surface of the block and a corresponding side. Etchant solutions which were less concentrated produced shallower trapezoidal or mesa shaped profiles at angles from about 10.degree. to 20.degree.. Such shallower profiles were probably a result of etching reactions being transport limited in the [111] B planes.

Detail Description Paragraph - DETX (48):

[0089] Higher concentrations of phosphoric acid (1:1:20 H.sub.2PO.sub.3:H.sub.2O.sub.2:H.sub.2O and above) created inward sloping (or reverse mesa) profiles limited by the reaction of the [111] B planes. Preferably, a phosphoric acid concentration (1:1:30 H.sub.2PO.sub.4:H.sub.2O.sub.2:H.sub.2O) between the dilute and concentrated solutions provides better profiles for assembly with recessed regions etched on the silicon substrate. Such etchant produced blocks having angles of 55.degree. parallel to the [110] plane and 49.degree. parallel to the [1[overscore (1)]0] plane, and typically etched the MBE grown layer at a rate of about 0.133 .mu.m/minute (or about 133 nm/min). In producing the results described, etchant **solution** was typically replenished when depleted.

Detail Description Paragraph - DETX (53):

[0094] After clearing off any oxide layers, a HF **solution** preferentially etched the sacrificial layer of aluminum arsenide to lift-off the gallium arsenide blocks. In particular, a HF **solution** having a concentration of about 5:1 H.sub.2O:HF was used to etch the sacrificial layer and lift off the blocks. Any blocks still remaining on the substrate possibly through surface tension can be mechanically removed from the substrate into a **solution**. Removed blocks include a base dimension of about 22 .mu.m by 23 .mu.m, compared to a designed dimension of 24 .mu.m by 24 .mu.m.

Detail Description Paragraph - DETX (54):

[0095] After removing the blocks from the substrate, a teflon pipet was used to remove a substantial portion of the HF **solution** from the gallium arsenide blocks. Any remaining HF was rinsed off with water. Such rinsing step created a mixture including blocks and water. An inert **solution** such as acetone then replaced the water to decrease any oxide formation on the blocks. Once in the inert **solution,** the blocks may cluster together and either float to the surface or settle to the bottom of the **solution**. Such clusters, often visible to the naked eye, decreased the effectiveness of a subsequent transferring step, and were therefore separated by mechanically agitating the **solution** with ultrasonic vibration.

Detail Description Paragraph - DETX (55):
[0096] The inert **solution** including gallium arsenide blocks was then transferred (or poured) evenly over the top surface of the silicon substrate. In particular, a pipet was used to transfer such **solution** over the top surface of the substrate. The **solution** is transferred at a rate creating substantially a laminar flow. Such laminar flow allowed the blocks to tumble and/or slide onto the top surface of the substrate and then self-align into the recessed regions via the trapezoidal profile. Generally, the transfer rate should provide an even flow of **solution** including blocks over the substrate surface but should not free or remove any blocks already disposed into the recessed regions.

Detail Description Paragraph - DETX (56):
[0097] Blocks fabricated by ion milling produced higher yields than wet etched blocks. Ion milled blocks having substantially consistent profiles self aligned and inserted into more than 90% of the recessed regions located on the substrate surface before the **solution** substantially evaporated. As the **solution** evaporates, surface tension often pulled a portion of the blocks out of the recessed regions. About 30% to 70% of the recessed regions remained filled after evaporation. The decrease in yield can be addressed by using liquids having lower surface tension during evaporation or by super critical drying methods which substantially eliminates surface tension. Alternatively, blocks may be bonded into the recessed regions prior to evaporation of the **solution,** thereby fixing the yield. Wet etched blocks having less consistent block profiles inserted correctly into about 1% to 5% of available recessed regions. Accordingly, ion milled blocks provided higher yields relative to the blocks fabricated by wet etching.

Detail Description Paragraph - DETX (64):
[0105] In creating silicon substrates having recessed regions for each silicon experiment, a **solution** of potassium hydroxide (KOH) produced recessed regions having a trapezoidal profile or inverted truncated pyramid shape. The **solution** created trapezoidal shaped profiles or inverted truncated pyramid

shapes having a larger face with lateral dimensions at the top surface with sides sloping inward at about 55.degree. from the top surface of the substrate. Trapezoidal profiles occurred due to the selectivity (1:200) between the [111] plane and the [100] plane. Specifically, the [111] plane etched slower than the [100] plane by the approximate ratio of 1:200.

Detail Description Paragraph - DETX (65):
[0106] In the silicon examples, the KOH **solution** etched trapezoidal recessed regions into about 500 .mu.m thick silicon wafers (5 cm.times.5 cm in overall area) using a mask consisting of rectangular openings. The KOH etchant **solution** used in the examples was a 1:2 (by weight) KOH:H.sub.2O **solution** at about 80.degree. C. Prior to the etching step, a silicon nitride (SiN.sub.x) mask layer was first formed on a top surface of such substrates.

Detail Description Paragraph - DETX (74):
[0115] The slowest etching planes for silicon in this KOH:H.sub.2O **etching solution** are the [111] planes, which can be considered etch stops forming the sloping sides of the shaped blocks. In each silicon experiment, the respective mask used to define the blocks must be aligned to the appropriate crystal axis. As shown in FIG. 100, a mask was used to form silicon trapezoidal shaped blocks. Trapezoidal shaped block is formed at the intersection of the diagonal lines on the mask. The width of the diagonal lines in the figure must be twice the thickness of the silicon block layer. For the larger trapezoidal blocks, a=0.2 mm and t=235 .mu.m; whereas, for the smaller trapezoidal blocks, a=0 and t=35 .mu.m.

Detail Description Paragraph - DETX (76):
[0117] In the first silicon experiment with the larger shaped blocks, the etched silicon wafer is placed in concentrated HF etch **solution** to remove the shaped blocks from contact with the SiN.sub.x sacrificial layer and any remaining SiN.sub.x from the mask layer. In the second silicon experiment with the smaller shaped blocks, the etched SOI wafer similarly is placed in concentrated HF etch **solution** to remove the shaped blocks from contact with the SiO.sub.2 sacrificial layer and any remaining SiN.sub.x from the mask layer. This HF etch **solution** preferentially etches the SiO.sub.2 and the SiN.sub.x to free the shaped blocks without etching the silicon shaped blocks. In particular, a HF **solution** having a concentration of about 1:1 HF:H.sub.2O was used to etch the sacrificial layer and residual SiN.sub.x to free the shaped blocks.

Detail Description Paragraph - DETX (77):
[0118] Once all the shaped blocks were free in the **solution,** the HF was

decanted and water was added. For the first silicon experiment, water and the larger shaped blocks formed the mixture or slurry. However, for the second silicon experiment, methanol and the smaller shaped blocks formed the mixture or slurry. As silicon is hydrophobic in nature, smaller shaped blocks having smaller mass tended to float on the surface of the water. The larger blocks did not have this problem because of their larger mass. Since methanol has both polar and nonpolar properties, the smaller shaped blocks did not float but preferably submerged into the fluid. As the silicon examples demonstrate, the selection of the fluid used in the slurry may depend on the mass of the shaped block, among other factors.

Detail Description Paragraph - DETX (82):

[0123] In order to achieve even higher fill-factors, especially for the smaller shaped blocks, care must be taken to properly etch the substrate and to keep the substrate and **solution** free of particles that could interfere with filling. For example, interference with filling could occur if the bottoms of the recessed regions are left rough by the KOH etching, or if particulates are deposited inside the recessed regions during the lapping process. Nonuniformity in the bottoms of the recessed regions could either prevent blocks from entering the recessed regions, or aid in the unfilling of the blocks from these recessed regions. Additionally, substrates with recessed regions that were not etched deep enough did not achieve high fill-factors, since the blocks protruding above the edge of the recessed region in the substrate could more easily be removed by fluid flow. Substrates with recessed regions that were etched too deeply also did not achieve high fill-factors. While the lateral dimensions at the top of an overetched recessed region remain the same, the lateral dimensions at the bottom of the recessed region become smaller as the depth is increased. Therefore, only the edges and not the smaller bottom face of a block filling an overetched recessed region will touch the substrate. Optimally, higher fill-factors are achieved when the recessed regions are neither underetched nor overetched.

Detail Description Paragraph - DETX (83):

[0124] Also described in general terms is the unique profiles for creating self-assembling devices. Such unique profiles, for example, are terms of a single block structure having a corresponding recessed region structure on a substrate for illustrative purposes only. The block structure may also include a variety of shapes such as a cylindrical shape, rectangular shape, square shape, hexagonal shape, pyramid shape, T-shape, kidney shape, and others. The block structure includes widths, lengths, and heights to promote self-assembly for a desired orientation. In addition, more than one type of structure may be present in the mixture (**solution** and blocks) as long as each structure includes a specific binding site on the substrate.